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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,060	02/26/2002	Kyle Spring	IR-1821 (2-2833)	4378

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,060	SPRING ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11 to 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *11 to 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Applicants' amendment filed on 09/30/2004 has been entered .

Therefore claims 11 and 18 as amended by the amendment and claims 12 to 17 as previously recited are currently pending in the Application.

Drawings

The corrected drawings received on 09/30/2004 are acceptable.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 to 18 are rejected under 35 U.S.C. 102 (b) as being obvious over Hshieh et al. (U.S. Patent No. 5,907,776, herein after Hshieh) previously applied and further in view of of Kumugai et al. (U.S. Patent No. 5,477,077 herein after Kumagai) or Baliga (U.S. Patent No. 4,969,028, herein after Baliga)

With respect to claim11 Hshieh describes a process for manufacturing a planar power semiconductor device comprising:

providing a semiconductor die including an epitaxially grown silicon layer of a first conductivity type formed over a substrate (Hshieh fig. 3 # 52, col. 4 lines 40-47) designating an active-area(Hshieh fig. 3 # 50, col. 4 lines 54-55) said active area being a portion of said epitaxially grown silicon layer in which channel regions are formed(Hsieh fig. 3 # 80) implanting dopants of a second conductivity in all of said active area of said epitaxially grown silicon layer ; (Hsieh col. 6 lines 55 61) forming a plurality of spaced channel regions of said second conductivity in said active area of said epitaxially grown silicon layer each channel region being spaced from another channel region by a first conductivity region in said epitaxially grown silicon layer ; (Hsieh figure 3 # 62) forming a source region of said first conductivity in

each of said channel regions, each source region being less wide and less deep than a channel region in which it is formed; (Hsieh figure 3 # 48, less wide/deep than 80)

Hsieh does not specifically describe forming a horizontally oriented gate structure over said epitaxially grown silicon layer and at least each lateral channel .

However Kumagai , a patent from the same filed of endeavor, describes in figure 3 and col.7 lines 30 to 35 describe forming a horizontally oriented gate structure over said epitaxially grown silicon layer and at least each lateral channel and in col. 11 lines 1 9 that vertical and horizontal devices can be interchangeable used and process steps to manufacture them are interchangeable to increase current gain and low gate power to turn-on without exhibiting the gate turn-off capability to form use the devices interchangeably and the at least process steps to manufacture them are interchangeable to form higher density-circuits and eliminate forming devices having problems associated with surface damage and contamination and also to reduce the leakage current in the devices, improve the speed of the device and increase current carrying capacity.

Therefore , it would have been obvious to one of ordinary skill in the art at the time of the invention to include Kumagi's teaching forming a horizontally oriented gate structure over said epitaxially grown silicon layer and at least each lateral channel and of vertical and horizontal devices can be interchangeable used and process steps to manufacture them are interchangeable. In Hsieh's method the motivation to make above substitution is to increase current gain and low gate power to turn-on without exhibiting the gate turn-off capability to form use the devices interchangeably and the at least process steps to manufacture them are interchangeable to form higher density-circuits and eliminate forming devices having problems associated with surface damage and contamination and also to reduce the leakage current in

the devices, improve the speed of the device and increase current carrying capacity.

Further, Baliga , also, in figures 4-5 and col. 2 lines 26 to line 68 describe the interchangeable use of vertical (grooved) and horizontal (planar) semiconductor devices in power devices like FETs to increase current gain and low gate power to turn-on without exhibiting the gate turn-off capability to form use the devices interchangeably and the at least process steps to manufacture them are interchangeable to form higher density-circuits and eliminate forming devices having problems associated with surface damage and contamination and also to reduce the leakage current in the devices, improve the speed of the device and increase current carrying capacity.

Therefore , it would have been obvious to one of ordinary skill in the art at the time of the invention to include Baliga's teaching of vertical and horizontal devices can be interchangeable used and process steps to manufacture them are interchangeable. In Hsieh's method . The motivation to make above substitution is to increase current gain and low gate power to turn-on without exhibiting the gate turn-off capability to form use the devices interchangeably and the at least process steps to manufacture them are interchangeable to form higher density-circuits and eliminate forming devices having problems associated with surface damage and contamination and also to reduce the leakage current in the devices, improve the speed of the device and increase current carrying capacity.

The remaining limitations of claim 11 are

wherein said first region of said epitaxially grown silicon is selected to cover an entire active region of said device. (Hsieh figure 3, Baliga figure 4, etc.).

With respect to claim 12 Hsieh describes a process according to claim 11, further comprising forming a field oxide termination structure at the edge of said active region prior to said implanting step.(Hsieh fig. 7 L # 56)

With respect to claim 13 Hsieh describes a process according to claim 11, further comprising forming a field oxide termination structure at the edge of said active region after said implanting step..(Hsieh fig. 7 L # 56). It is noted that selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhaus, 154 F.2d. 690, 69 USPQ 330 (CCPA1946) , see also Ex parte Rubin, 126 USPQ 440 (BAPH959).

With respect to claim 14 Hsieh describes a process according to claim 11, wherein said gate structure comprises a gate oxide, said gate oxide being formed after said implanting step. (Hsieh fig. 7 N).

With respect to claim 15 Hsieh describes a process according to claim 12, wherein said field oxide is formed over said epitaxially grown silicon and etched to provide a window over said first region, wherein said dopants of said second conductivity are implanted through said window.(Hsieh figs. 71 and 7 L)

With respect to claim 16 Hsieh describes a process according to claim 11, wherein said dopants of said second conductivity are comprised of boron. (Hsieh figure 7 I B)

With respect to claim 17 Hsieh describes a process according to claim 11, wherein said dopants of said second conductivity type are comprised of either arsenic or phosphorous. (Hsieh figure 7 L P).

With respect to claim 18. Hsieh describes a process according to claim 11, further comprising, forming an oxide interlayer over said gate structure, opening windows in said oxide

inter layer over at least said source regions; and forming a source contact over said oxide interlayer and a heavy base region. (Hsieh figure 7N and M # 58).

Response to Arguments

Applicant's arguments filed October 07, 2004 have been fully considered but they are not persuasive for the following reasons

Applicants' first contention that the applied reference's (i.e. Hsieh's) teachings should be limited to lateral gate structure over lateral channel is moot in view of the newly applied references.

Applicants' second contention that Hshieh does not teach the step of implanting dopants of a second conductivity type in all of the active area prior to forming channel region is not persuasive for several reasons.

First Applicants' claim language recites " comprising", an open ended term therefore the order of performing the steps is not recited. therefore Applicants' arguments are not commensurate in scope with presently recited claims.

Secondly Applicants' arguments are based incomplete analysis Of Hshieh's teachings. Hshieh in figure 7 I reproduced below shows second implant (P type; first implant was N type) before the formation of spaced channel region of second conductivity type which is formed in figure 7L .(see patent).

Further proof that Hshieh shows blanket implantation at least in figures 7 I and J and col. 7 lines 34-38 (reproduced below) which steps occur prior to forming other features of the device (see features formed in figures 7 L to 7 N) (are :

Therefore Hshieh and Kumugai and/or Baliga render obvious claims 11 to 18.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

January 06, 2005

PHAT X. CAO
PRIMARY EXAMINER